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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,447	12/23/1999	ROBERT BEDICHEK	TRANS18	7416

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EXAMINER
DAY, HERNG DER

ART UNIT	PAPER NUMBER
2123	14

DATE MAILED: 08/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/471,447	BEDICHEK ET AL.	
	Examiner	Art Unit	
	Herng-der Day	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This communication is in response to Applicants' Supplemental Amendment (paper # 13) to Office Action dated March 25, 2003 (paper # 9), mailed June 16, 2003.

1-1. Claims 1-15 have been cancelled; claims 16-32 have been added; claims 16-32 are pending.

1-2. Claims 16-32 have been examined and claims 16-32 have been rejected.

Drawings

2. The drawings are objected to for the following reasons. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2-1. As described in the specification, lines 14-15 of page 4, "The microprocessor pictured is described in detail in U. S. patent 5,832,205". Therefore, Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

2-2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

(a) microprocessor 11, as described in line 13 of page 4.

2-3. Figure 4 has not been referenced in the "Detailed Description" of the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 16-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Kelly et al., U.S. Patent 5,832,205 issued November 3, 1998 (IDS, paper # 11, No. C).

4-1. Regarding claim 16, Kelly et al. disclose a method of determining validity of a translated instruction comprising:

a) starting execution of a first host instruction translated from a first target instruction, wherein said first host instruction is linked from a second host instruction translated from a second target instruction, and wherein a first condition of a target system state required by said first host instruction holds (execution, column 23, lines 1-29);

b) testing a second condition of said target system state to determine the validity of said first host instruction (condition of the T bit, column 23, lines 7-9);

c) executing said first host instruction if said second condition holds; and d) generating an exception if said second condition does not hold (if an attempt to write to the target address occurs, the attempt generates an exception, column 23, lines 29-35).

4-2. Regarding claim 17, Kelly et al. further disclose said first condition is based on an address consistency check of said second host instruction (condition of the A/N bit, column 23, lines 10-12).

4-3. Regarding claim 18, Kelly et al. further disclose said b) comprises performing an address consistency check of said first host instruction (condition of the T bit, column 23, lines 7-9).

4-4. Regarding claim 19, Kelly et al. further disclose said b) comprises performing an address consistency check of said first host instruction (condition of the T bit, column 23, lines 7-9).

4-5. Regarding claim 20, Kelly et al. further disclose said d) further comprises invalidating said first host instruction (invalidated, column 23, lines 32-35).

4-6. Regarding claim 21, Kelly et al. further disclose said d) further comprises removing said link between said first host instruction and said second host instruction (committed original state may be recalled, column 12, line 66, through column 13, line 5).

4-7. Regarding claim 22, Kelly et al. further disclose said d) further comprises creating a new translation of said first target instruction (generation of new translations, column 13, line 65, through column 14, line 2).

4-8. Regarding claim 23, Kelly et al. further disclose said d) further comprises interpreting said first target instruction (uncommitted memory stores may be dumped, column 12, line 66, through column 13, line 5).

4-9. Regarding claim 24, Kelly et al. disclose a method of determining validity of a translated instruction comprising:

a) performing a first address consistency check of a first host instruction made from a first target instruction to verify that said first host instruction is valid (condition of the T bit, column 23, lines 7-9);

b) executing said first host instruction (execution, column 23, lines 1-29);

c) determining whether a second host instruction made from a second target instruction and that is linked from said first host instruction can be safely executed without a second address consistency check; and d) executing said second host instruction without performing said second address consistency check if safe (committed to memory, column 17, lines 1-39).

4-10. Regarding claim 25, Kelly et al. further disclose comprising:

e) performing said second address consistency check if said determination is that it is unsafe to execute said second host instruction without said second address consistency check (condition of the T bit, column 23, lines 7-9); and

f) executing said second host instruction (execution, column 23, lines 1-29).

4-11. Regarding claim 26, Kelly et al. further disclose said c) is implied from said first address consistency check (the condition of the T bit indicating whether a translation has been accomplished for the target instruction is detected, column 23, lines 7-9).

4-12. Regarding claim 27, Kelly et al. further disclose multiple target instructions are translated to host instructions (subsequent target instructions, column 23, lines 15-18) and wherein said c) comprises determining whether any of said target instructions reside on different pages of memory (Compare, Fig 11).

4-13. Regarding claim 28, Kelly et al. further disclose multiple target instructions are translated to host instructions (subsequent target instructions, column 23, lines 15-18) and wherein said c) comprises determining whether any of said target instructions reside on different pages of memory (Compare, Fig 11).

4-14. Regarding claim 29, Kelly et al. disclose a method of linking translated instructions comprising:

a) translating a first target instruction to a first host instruction (first three instructions in the sample, column 25);

b) determining that said first host instruction is to be linked to a second host instruction translated from a second target instruction (next three instructions in the sample, column 25); and

c) providing an address consistency check for said first host instruction (instructions chkl and chku in the sample, column 26).

4-15. Regarding claim 30, Kelly et al. further disclose:

said b) comprises determining at the time said translation of said first target instruction is made that said first and second host instructions are to be linked (sample, column 26); and

said c) comprises:

c1) linking said second host instruction to said first host instruction (sample, column 26; adding the second host instruction "mov" after the first host instruction "mov"); and

c2) including code for performing said address consistency check as a part of said first host instruction (sample, column 26; including instructions "chkl" and "chku" to the first host instruction "mov").

4-16. Regarding claim 31, Kelly et al. further disclose:

said b) comprises determining after said translation of said first target instruction is made that said first and second host instructions are to be linked (sample, column 25); and

said c) comprises:

c1) linking said second host instruction to code for performing said address consistency check (sample, column 26; attaching the second host instruction "mov" to instructions "chkl" and "chku"); and

c2) linking said code for performing said address consistency check to said first host instruction (sample, column 26; attaching instructions "chkl" and "chku" to the first host instruction "mov").

4-17. Regarding claim 32, Kelly et al. further disclose:

said b) comprises determining after said translation of said first target instruction is made that said first and second host instructions are to be linked (sample, column 25); and

said c) comprises:

c1) linking said second host instruction to said first host instruction (sample, column 26; adding the second host instruction "mov" after the first host instruction "mov"); and

c2) incorporating code for performing said address consistency check into said first host instruction (sample, column 26; incorporating instructions "chkl" and "chku" to the first host instruction "mov").

Conclusion

5. The prior art made ~~of record and not relied upon is considered pertinent to~~ applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Herng-der Day whose telephone number is (703) 305-5269. The examiner can normally be reached on 8:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day
August 22, 2003

HUGH JONES, Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100